U_LOGIC_FPGA
LOGIC_FPGA.SchDoc

U_DIGITAL_IO
DIGITAL_IO.SchDoc

U_PERIPHERAL_PORT_IO
PERIPHERAL_PORT_IO.SchDoc

U_RAM
RAM.SchDoc

U_POWER_SUPPLY
POWER_SUPPLY.SchDoc

U_FPGA_POWER_AND_CONFIGURATION
FPGA_POWER_AND_CONFIGURATION.SchDoc

SCRW1
SCRW - 4-40x1/4-Nylon
SCRW2
SCRW - 4-40x1/4-Nylon
SCRW3
SCRW - 4-40x1/4-Nylon
SCRW4
SCRW - 4-40x1/4-Nylon

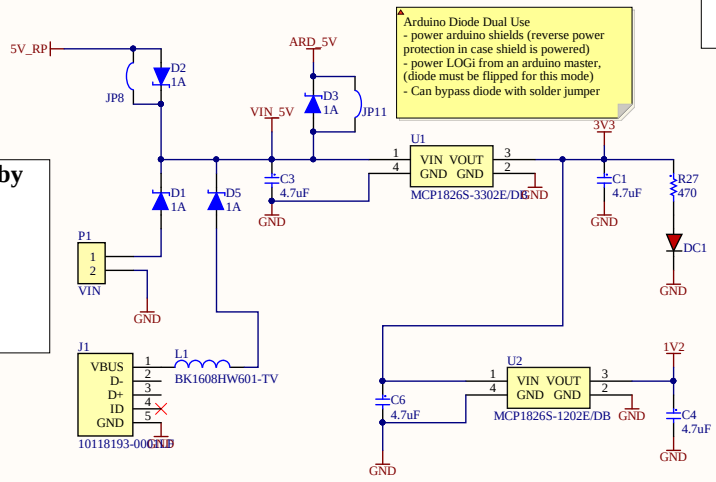
STDOFF1
STDOFF - 4-40-5/8"
STDOFF2
STDOFF - 4-40-5/8"

M1
Rubber Bumper
Rubber Bumper Standoff

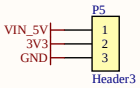
Title	LOGi-Pi Top Level		
Revision:	R1.5	Sheet	1 of 7
Date:	3/20/2017	Engineer:	Michael Jones

ValentFX
ELECTRONICS INNOVATION

Power: By Default Power will be supplied by the .
Raspberry Pi
Optionally power can be supplied through FPGA VIN header.



1 x Auxillary Power output Header

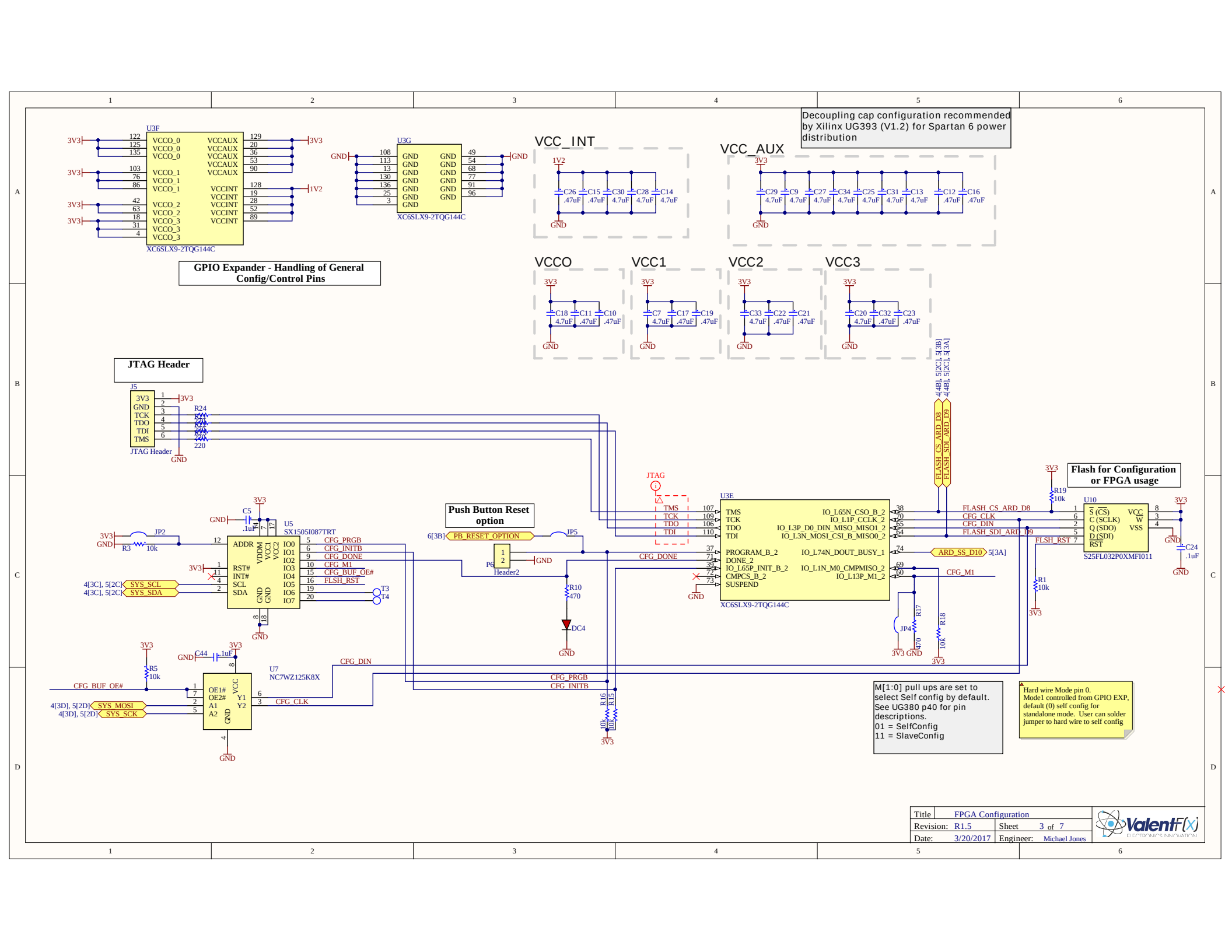


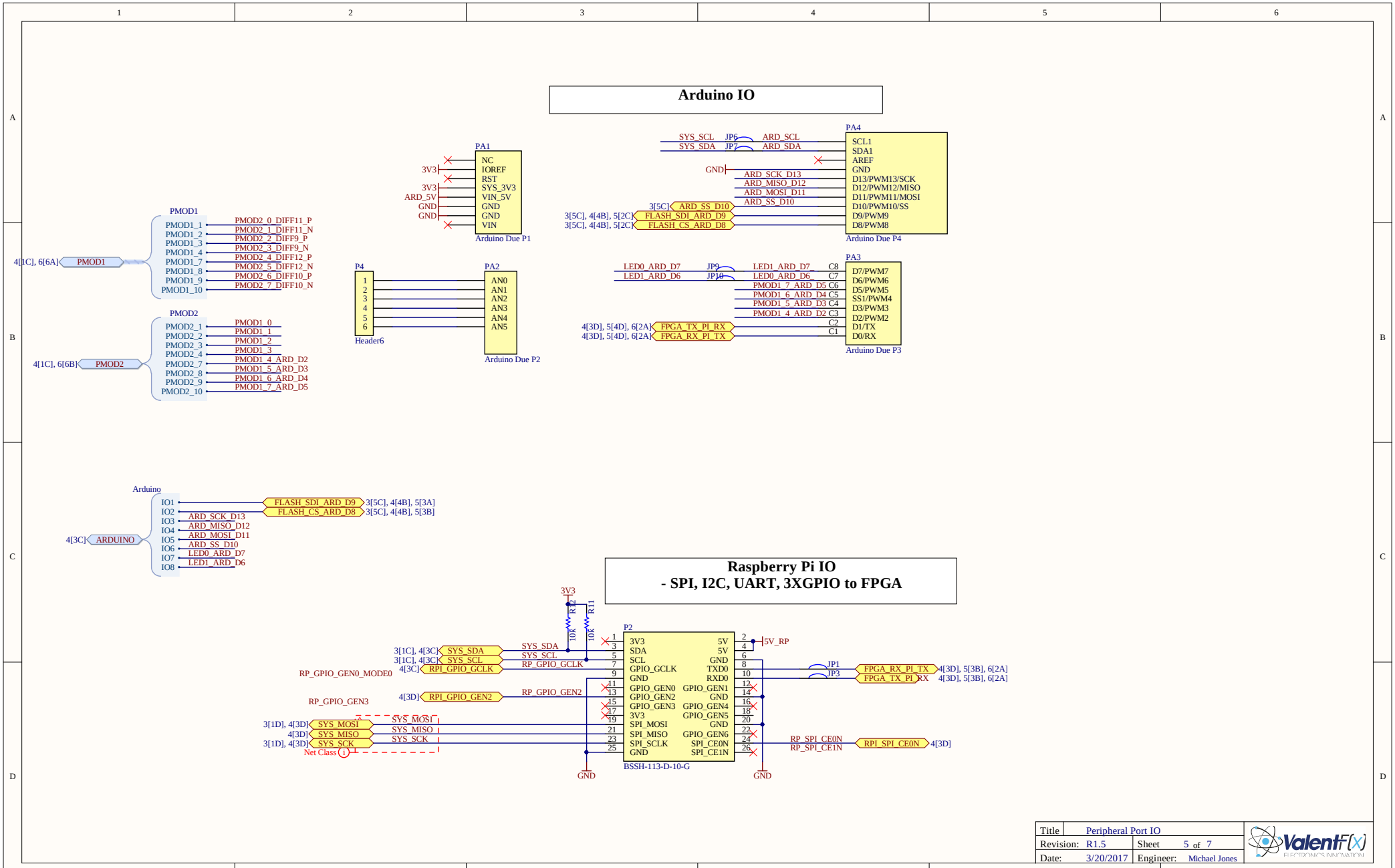
LOGI-LOGO
LOGO1

VALENTFX-LOGO-500
Logo2

VALENTFX-LOGO-750
Logo3

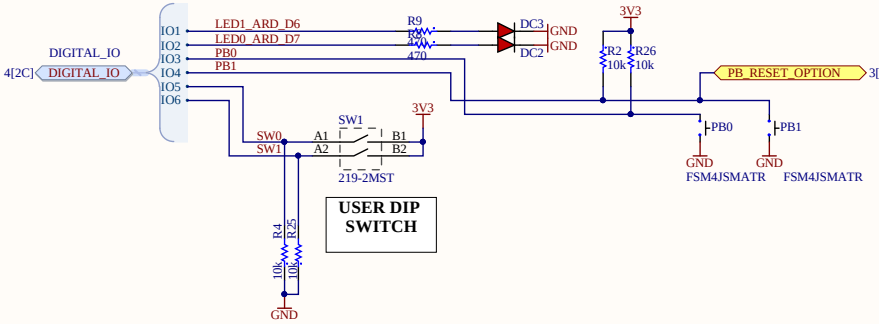
Title	Power Supply		
Revision:	R1.5	Sheet	2 of 7
Date:	3/20/2017	Engineer:	Michael Jones


Decoupling cap configuration recommended by Xilinx UG393 (V1.2) for Spartan 6 power distribution
VCC_INT
VCC_AUX
VCCO
VCC1
VCC2
VCC3
GPIO Expander - Handling of General Config/Control Pins
JTAG Header
Push Button Reset option
Flash for Configuration or FPGA usage
M[1:0] pull ups are set to select Self config by default. See UG380 p40 for pin descriptions.
01 = SelfConfig
11 = SlaveConfig
Hard wire Mode pin 0. Mode1 controlled from GPIO EXP, default (0) self config for standalone mode. User can solder jumper to hard wire to self config
Title FPGA Configuration
Revision: R1.5
Sheet 3 of 7
Date: 3/20/2017
Engineer: Michael Jones



Title	Peripheral Port IO		
Revision:	R1.5	Sheet	5 of 7
Date:	3/20/2017	Engineer:	Michael Jones

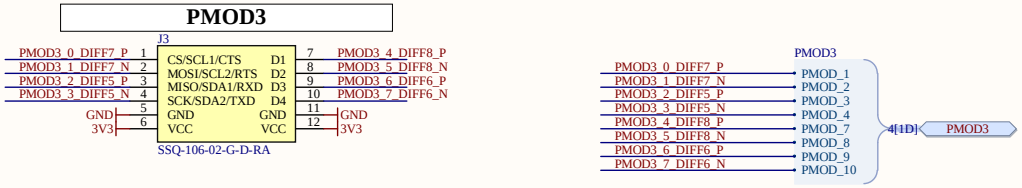
DIGITAL IO

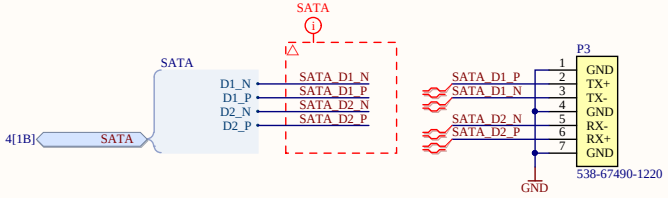


PMOD1

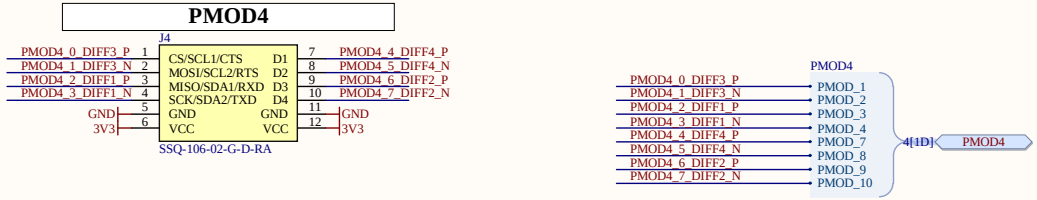
PMOD2

PMOD3



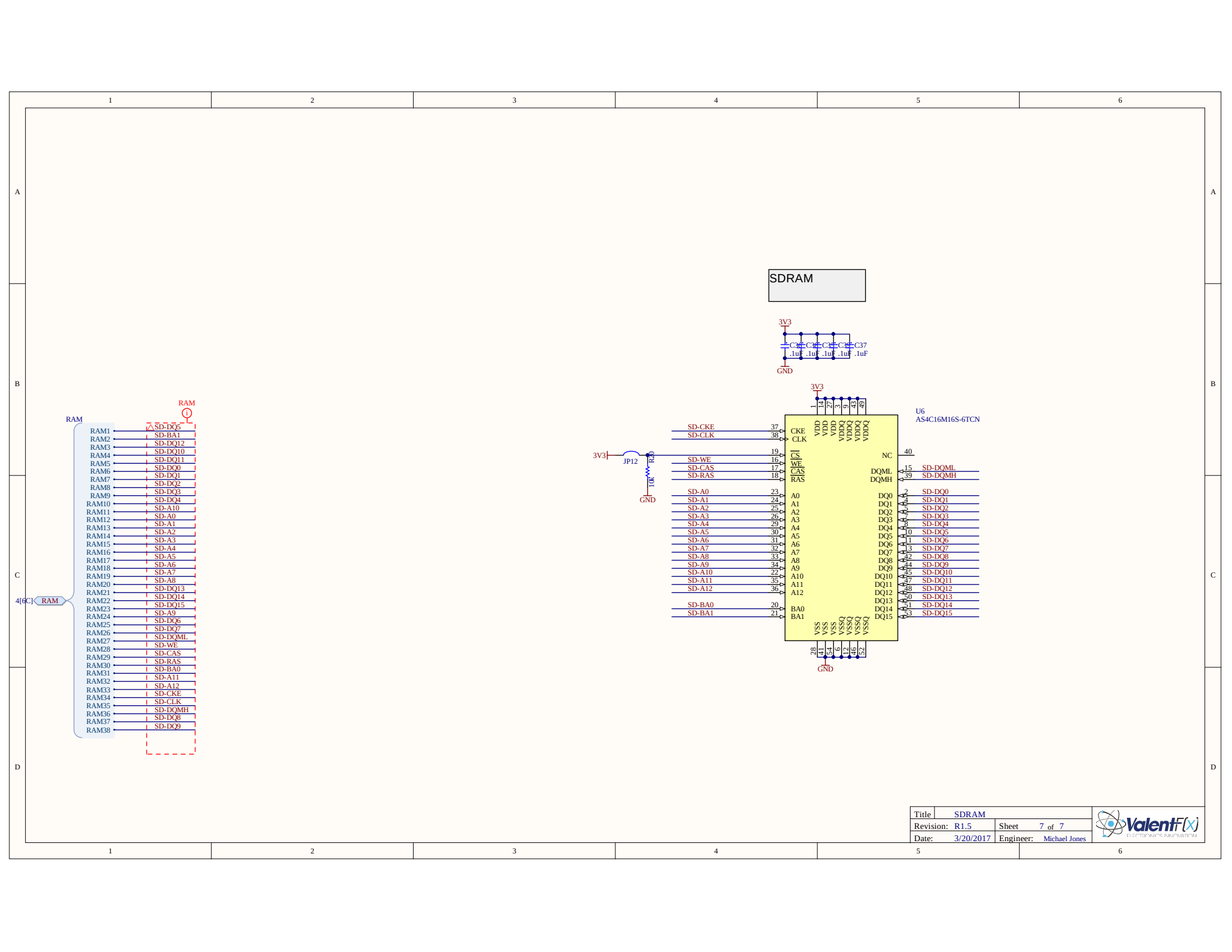


PMOD4



Title	Digital IO		
Revision:	R1.5	Sheet	6 of 7
Date:	3/20/2017	Engineer:	Michael Jones

ValentFX ELECTRONICS INNOVATION


SDRAM
3V3
C36 .1uF
C34 .1uF
C35 .1uF
C38 .1uF
C37 .1uF
GND
U6
AS4C16M16S-6TCN
VDD
VDDQ
CKE
CLK
CS
WE
CAS
RAS
DQML
DQMH
NC
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
BA0
BA1
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
VSS
VSSQ
SD-CKE
SD-CLK
SD-WE
SD-CAS
SD-RAS
SD-A0
SD-A1
SD-A2
SD-A3
SD-A4
SD-A5
SD-A6
SD-A7
SD-A8
SD-A9
SD-A10
SD-A11
SD-A12
SD-BA0
SD-BA1
SD-DQML
SD-DQMH
SD-DQ0
SD-DQ1
SD-DQ2
SD-DQ3
SD-DQ4
SD-DQ5
SD-DQ6
SD-DQ7
SD-DQ8
SD-DQ9
SD-DQ10
SD-DQ11
SD-DQ12
SD-DQ13
SD-DQ14
SD-DQ15
JP12
R20
10K
RAM
RAM1
RAM2
RAM3
RAM4
RAM5
RAM6
RAM7
RAM8
RAM9
RAM10
RAM11
RAM12
RAM13
RAM14
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RAM16
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RAM26
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RAM31
RAM32
RAM33
RAM34
RAM35
RAM36
RAM37
RAM38
SD-DQ5
SD-BA1
SD-DQ12
SD-DQ10
SD-DQ11
SD-DQ0
SD-DQ1
SD-DQ2
SD-DQ3
SD-DQ4
SD-A10
SD-A0
SD-A1
SD-A2
SD-A3
SD-A4
SD-A5
SD-A6
SD-A7
SD-A8
SD-DQ13
SD-DQ14
SD-DQ15
SD-A9
SD-DQ6
SD-DQ7
SD-DQML
SD-WE
SD-CAS
SD-RAS
SD-BA0
SD-A11
SD-A12
SD-CKE
SD-CLK
SD-DQMH
SD-DQ8
SD-DQ9
4[6C]
Title SDRAM
Revision: R1.5
Sheet 7 of 7
Date: 3/20/2017
Engineer: Michael Jones
ValentFX
ELECTRONICS INNOVATION

PCB Fabrication Notes

Unless otherwise specified, all dimensions are in inches
Overall Dimension: 3.471" x 2.685"
Finished Thickness: .062"
Layer Count: 4
Min Thru Hole: 13 mil
Annular Ring: 7 mil
Min Trace/Space: 6 mil
Drill Count: 569
PAD Count: 579
Component Count: 116
Via Count: 433

Plating: Gold ENIG
Solder Mask: Black
Legend: White Non-Conductive Ink LPI Process
RS274-X Gerber Format, 2,5 Leading Zeros Suppressed
Excellon Drill Format, 2,5 Trailing Zeros Suppressed

Layer Details: 4-Layer Stackup	POLARITY
✓GTL - Top Copper	POSITIVE
✓G1 - Inner Copper (Ground)	POSITIVE
✓G2 - Inner Copper (VDD)	POSITIVE
✓GBL - Bottom Copper	POSITIVE

✓GTO - Top Silkscreen
✓GBO - Bottom Silkscreen
✓GTP - Top Solder Paste
✓GBP - Bottom Solder Paste
✓GTS - Top Solder Mask
✓GBS - Bottom Solder Mask
✓GKO - Board Outline
✓GM1 - 3D Part Bodies - System
✓GM2 - Board Dimensions
✓GM3 - Single Board Fabrication Notes
✓GM4 - Single Board Score/Tab Route
✓GM13 - 3D Body All
✓GM15 - Assembly Outlines - Top
✓GM20 - Panel Dimensions
✓GM21 - Panel Score/Tab Route
✓GM22 - Panel Dimensions

.TXT/.DRL - NC-Drill